



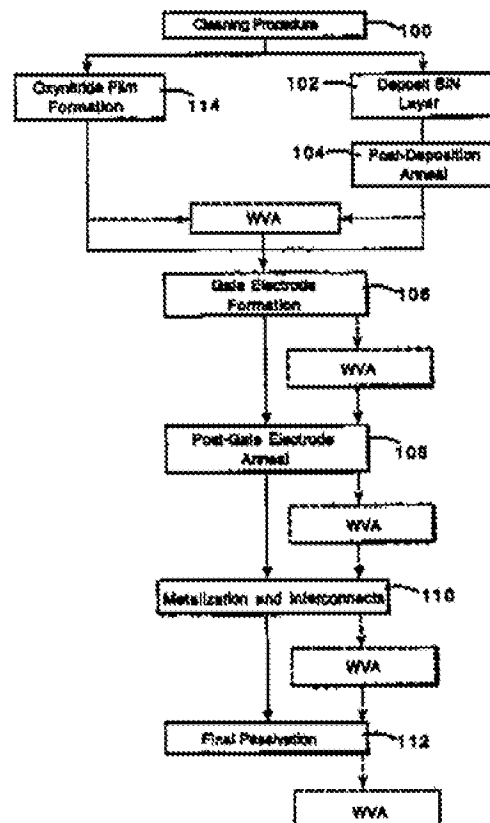
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H01L	A2	(11) International Publication Number: WO 97/25738 (43) International Publication Date: 17 July 1997 (17.07.97)
(21) International Application Number: PCT/US97/00217 (22) International Filing Date: 6 January 1997 (06.01.97) (30) Priority Data: 08/583,640 5 January 1996 (05.01.96) US (71) Applicant: YALE UNIVERSITY [US/US]; 451 College Street, New Haven, CT 06520 (US). (72) Inventor: WANG, Xie, Wen; 400 Haysick Hill Road, Orange, CT 06477 (US). (74) Agent: PRAHL, Eric, L.; Fish & Richardson P.C., 225 Franklin Street, Boston, MA 02110-2804 (US).		(81) Designated States: AU, CA, JP, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>Without international search report and to be republished upon receipt of that report.</i>

(54) Title: A WATER VAPOR ANNEALING PROCESS

(57) Abstract

A method of fabricating semiconductor devices including the steps of forming a silicon-based dielectric layer containing nitrogen having a concentration that is in a range of a fraction of a percent up to stoichiometric Si_3N_4 ; and annealing the dielectric layer in a water vapor atmosphere.



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A WATER VAPOR ANNEALING PROCESSBackground of the Invention

5 The invention relates generally to a process for improving the electrical characteristics of semiconductor devices which employ silicon nitride and/or silicon oxynitride layers.

 A typical fabrication sequence of the silicon
10 nitride (or oxynitride) gate dielectric involves: (1) cleaning of Si wafer; (2) forming silicon nitride (or oxynitride) on Si wafer; (3) performing a post-deposition high-temperature anneal in nitrogen or oxygen and typically at temperatures $>800^{\circ}\text{C}$; (4) depositing a gate
15 electrode; and (5) performing a post-gate electrode anneal in nitrogen or forming gas, typically between 400°C and 500°C . A variety of dielectric deposition methods have been used in the past, including APCVD, LPCVD, PECVD, and JVD.

20 In addition to deposition, the silicon oxynitride mentioned above may be formed by nitridizing a thermal oxide layer at an elevated temperature in N_2O or NH_3 ambient, or by directly oxidizing Si in an N_2O ambient, or by reoxidizing a silicon nitride or oxynitride film, etc.

25 Relative to silicon dioxide, silicon nitride or silicon oxynitride possesses a number of attractive features as a gate dielectric for Field Effect Transistors (FET's), including (1) higher dielectric constant, (2) better barrier against impurity diffusion,
30 and (3) better resistance to radiation damage and hot-carrier damage. Unfortunately, the electrical properties of the silicon/nitride interface are very poor due to the presence of very high densities of interface

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traps and bulk traps. Therefore, numerous attempts have been made by various research groups over the past 3 decades to improve the electrical properties of the silicon nitride layer and thereby produce FET's which
5 out-perform conventional MOSFET's using silicon dioxide as the gate dielectric. However, none of these efforts has been truly successful.

Summary of the Invention

In one aspect, the invention involves inserting a
10 new process step in the fabrication of Metal-Insulator-Semiconductor Devices (MIS's) that contain silicon nitride or silicon oxynitride in their gate dielectrics, where the silicon oxynitride may contain as little as a fraction of a percent of nitrogen. For brevity, such
15 devices will be called MNS devices in this document. This new process dramatically improves the performance of a variety of MNS devices.

The new process step is: (1) a water-vapor annealing treatment after the formation of the gate
20 dielectric (i.e., after step 3 above); or (2) a water-vapor annealing treatment which replaces the conventional post-gate electrode annealing treatment (i.e., step 5 above); or (3) a water-vapor annealing treatment after subsequent metalization steps, or (4) a combination of
25 the above. The water-vapor anneal may be performed at a temperature in the range of about 270-500°C for 30 min. (approx.). The results of performing such a water-vapor anneal are remarkable. It greatly reduces the density of interface traps and it greatly enhances channel mobility
30 in MNS devices, to the point that MNS devices should be commercially viable.

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In general, in one aspect, the invention is a method of fabricating semiconductor devices including the steps of forming a silicon-based dielectric layer containing nitrogen having a concentration that is in a
5 range of a fraction of a percent up to stoichiometric Si_3N_4 ; and annealing the dielectric layer in a water vapor atmosphere.

Preferred embodiments have the following features. The method further includes the step of forming a gate-
10 electrode on the dielectric layer. The water vapor anneal step is performed after forming the gate-electrode. alternatively, the water vapor anneal step is performed before forming the gate-electrode. The dielectric layer is made of silicon nitride, or silicon
15 oxynitride, or a nitrided silicon oxide, or a nitrodized silicon oxide. the water vapor anneal step is performed at a temperature which is in the range of about 270°C to 500°C.

In general, in another aspect, the invention is a
20 semiconductor device fabricated in accordance with the above-described procedure (i.e., using a WVA step).

In general, in yet another aspect, the invention is a method of fabricating semiconductor devices including the steps of forming a dielectric layer made of
25 a material that is selected from a group of materials consisting of silicon nitride, silicon oxynitride, nitrided oxide, and nitrodized oxide; annealing the dielectric layer in a water vapor atmosphere.

In general, in still another aspect, the invention
30 is a method of improving electrical characteristics of a metal-insulator-semiconductor (MIS) device in which the insulating layer comprises a dielectric selected from the group of materials consisting of silicon nitride, silicon

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oxynitride, nitrided oxide, and nitrodized oxide. the method includes the step of annealing the device in a water vapor atmosphere.

The use of water vapor at a modest annealing temperature in the nitride fabrication process "passivates" the nitride/Si (or oxynitride/Si) interface. The advantage over the present technology is that it enables high-quality MOSFET's to be fabricated. The invention can be used in the fabrication of all semiconductor devices and IC's containing a silicon nitride or nitrided silicon oxide layer where the electrical properties of that layer and its interfaces are of concern. For example, it can be used to improve the performance and characteristics of: (1) gate dielectrics of FET's used in microprocessors, DRAMs, SRAMs, Flash Memories, and EEPROMs, just to name a few; (2) dielectrics for storage capacitors in DRAMs; (3) inter-poly dielectrics; and (4) thin-film transistors (used in SRAMs and flat panel display technologies, for example.)

Other advantages and features will become apparent from the following description of the preferred embodiment and from the claims.

Brief Description of the Drawings

Fig. 1 shows a representative fabrication sequence that has been modified in accordance with the invention;

Fig. 2 is a plot of the quasi-static capacitance versus gate voltage for two MNS capacitors, one fabricated using the water-vapor anneal step (B) and the other fabricated without benefit of a water-vapor anneal step (A);

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Fig. 3 shows a plot of capacitance versus gate voltage for the capacitor of curve B in Fig. 2 after it has had a further water-vapor anneal step performed as a post-gate electrode-anneal;

5 Fig. 4 is a plot of leakage current for two devices, one fabricated using the water-vapor anneal and the other fabricated without it;

Fig. 5 is a plot of the transconductance (G_m) of:
(1) a control MOSFET (dashed curve); (2) a MOSFET with N_2O
10 oxynitride without WVA treatment (lower solid); and (3)
MOSFET with N_2O oxynitride with WVA treatment (upper
solid);

Fig. 6 is a plot of the peak transconductance versus channel length for two sets of MOSFET's with an N_2O
15 annealed gate oxide, one of which benefitted from the WVA and the other of which did not; and

Fig. 7 are plots of charge pumping current versus gate voltage for: (I) a MOSFET having an N_2O oxynitride as gate dielectric with no WVA treatment; (II) same device
20 with WVA; (III) control device with oxide as gate dielectric.

Description of the Preferred Embodiments

I have discovered that performing a water-vapor anneal on silicon nitride or silicon oxynitride layers
25 substantially improves the quality of the devices. Experiments have been conducted which dramatically showed the benefits of adding such an anneal to the fabrication procedure.

For some of the experiments that are reported
30 herein, we started with (100) oriented Si wafers which had a resistivity of about a few ohm-cm. We processed these substrates to fabricate metal-nitride-silicon

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capacitors using standard fabrication procedures. First, we performed a standard cleaning procedure to produce very clean bare silicon wafers with no native oxide on its surfaces (step 100). These wafers were then loaded
5 into a silicon nitride deposition chamber. We deposited a silicon nitride film on the silicon substrate (step 102). The layers that were deposited were about 80-90Å which is electrically equivalent to a SiO₂ layer of about 40-45Å. After deposition, we transferred the wafer from
10 the nitride deposition chamber to a furnace for post-deposition annealing at 800°C for 30 minutes in a dry N₂ ambient (step 104).

We followed the post-deposition anneal with an aluminum evaporation and then used standard
15 photolithography procedures to form the gate electrodes (i.e., the top electrodes) of the MNS capacitors (step 106). Then, we performed another aluminum evaporation on the backside of the wafers, thereby forming the other electrode of the MNS capacitors. Finally, we performed a
20 post-electrode anneal in N₂ or forming gas (step 108).

Typically, the process might further include a phase during which metalizations and interconnects are formed for the devices (step 110) and then the chip is passivated by applying a passivation layer (e.g. SiN)
25 (step 112).

Note that the procedure just described also generally describes the formation of devices which utilize an oxynitride layer for the dielectric, except that instead of using deposition equipment to form a SiN
30 layer other fabrication equipment is used to form the dielectric layer. This is illustrated by the alternative path through box labeled 114.

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In this general process, we inserted a water vapor anneal (WVA) step. We found that the WVA step can be inserted either before or after the electrode formation steps. The alternative locations for the WVA step are 5 represented in Fig. 1 by the dashed boxes. Regardless of where the WVA step was inserted, it dramatically improved device performance.

We performed the WVA step in a standard steam oxidation furnace such as is typically found in many 10 wafer fabrication facilities. The furnace tube which was at 380°C and the total WVA anneal time was about 30 minutes. During the WVA anneal, we supplied water vapor to one end of the tube simply by using an infra-red lamp to heat up a tank of deionized (DI) water that was 15 connected to the tube. The heated DI water evaporated and flowed through the tube and over the devices that were being annealed.

We fabricated two sets of MNS capacitors, one set made by using a post-deposition WVA and the other set 20 made without any WVA. In both sets, the dielectric (i.e., the silicon nitride layer) had an equivalent oxide thickness of about 5.3 nm (nanometers). We compared the electrical characteristics of devices from both sets. For example, we measured quasi-static capacitance versus 25 gate voltage for devices from each set (see the curves shown in Fig. 2). Curve A represents the performance of a device which was made without using a post-deposition WVA and Curve B represents the performance of a device that was made with a post-deposition WVA. As can be 30 seen, there is a marked reduction in quasi-static capacitance for the device that benefitted from the WVA.

Referring to Fig. 3, the capacitor represented by curve B in Fig. 2 then received a WVA treatment again as

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a post-metal anneal and the high frequency and quasi-static capacitance versus voltage (C-V) curves were measured for this device. As can be seen, the high frequency C-V (HFCV) and the quasi-static CV curves
5 perfectly match over much of the accumulation and depletion regions. This indicates a very low density of interface states. In addition, the measured flatband voltage of HFCV also indicated a low density of dielectric charge.

10 We also measured the impact of a WVA on leakage current in devices that had 2 mil diameter electrodes and an effective oxide thickness of about 47\AA . These results are shown in the I_g versus V_g curves of Fig. 4. The curve on the left is I_g - V_g before WVA and the curve on the right
15 is after WVA. Again, a post-deposition WVA treatment significantly reduces leakage current.

We also evaluated the impact of the WVA on the electrical performance of MOSFET's that were fabricated and supplied by a third party. These MOSFET's had an N_2O
20 oxynitride layer as the gate dielectric. The oxynitride films were formed by either annealing a previously formed SiO_2 layer in an N_2O ambient or by oxidizing Si directly in an N_2O ambient. Their thicknesses were approximately 80\AA , and they contain small amounts of nitrogen, ranging
25 from a fraction of a percent to a few percent. Fig. 5 shows the how much transconductance (G_m) improves when the WVA is used. The lower solid curve shows the performance of the MOSFET without using a WVA and the upper solid curve shows the performance of the MOSFET
30 after using a WVA. The dashed line represents data from a control sample, which used a thermal oxide as a gate dielectric rather than a N_2O oxynitride. As can be seen, the G_m values of the WVA treated device are far superior

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to those of the untreated device. In fact, the peak G_m value of WVA treated device is as good as that of the control sample and in the high field range, the G_m values are much superior even to that of the control sample.

5 Referring to Fig. 6, a plot of the peak transconductance versus channel length also shows a similar consistent and substantial improvement from the WVA. The upper curve is for devices that benefitted from the WVA and the lower curve is for devices that did not
10 use the WVA. In general, the WVA produces about a 10-20% increase in peak transconductance.

We measured charge pumping current of the various devices and found that the WVA produced a drastic decrease in charge pumping current. This is strong
15 evidence that the improvement that we have seen in the other measurements is due to a reduction in interface trap density and oxide charge. Fig. 7 shows three curves of charge pumping current versus gate voltage. The top curve is for a N_2O oxynitride MOSFET device which was not
20 given a WVA treatment; the bottom curve is for the same device after it was given a WVA treatment; and for comparison purposes, the middle curve is for a MOSFET that used a thermal oxide (i.e., SiO_2) as the gate-dielectric.

25 We observed a positive effect over a temperature range of 270-500°C, with the best results occurring at about 380°C. We expect, however, that as further experiments are performed, we will see the beneficial effect of the WVA under other process conditions and at
30 temperatures outside of this range.

The nitride or oxynitride may be formed by any number of ways, including chemical vapor deposition, physical vapor deposition, or by nitriding thermal SiO_2

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(e.g. by introducing a fraction of a percent to a few percent of nitrogen into SiO_2 by annealing SiO_2 in N_2O or NH_3 ambient at high temperatures). It is not intended that the invention be limited in any way with regard to
5 how the SiN or silicon oxynitride layer is formed.

The WVA step has been inserted at various locations into the fabrication process, all producing positive results. The following illustrates the variety of ways in which the WVA step was inserted into the
10 fabrication procedure:

- (1) nitride (or oxynitride) formation + WVA + high-temperature (e.g. $\sim 800^\circ\text{C}$) N_2 anneal + gate electrode deposition + post-gate electrode annealing @ 400°C
 - 15 (2) nitride (or oxynitride) formation + high-temperature N_2 anneal + WVA + gate electrode deposition + post-gate electrode annealing
 - (3) nitride (or oxynitride) formation + high-temperature N_2 anneal + gate electrode deposition
20 + WVA (to replace post-gate electrode annealing)
 - (4) nitride (or oxynitride) formation + high-temperature N_2 anneal + WVA + gate electrode deposition + WVA (to replace post-gate electrode annealing)
- 25 Though all of the above-described combinations produced positive results, the last one tended to produce the best results.

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Though we have described specific process steps and structures for which our experiments were performed, the invention is not limited to such process steps or to such structures. For example, though we used

5 metalizations to form the gate electrodes in our experiments, today such electrodes are more typically formed by polysilicon layers. The invention is not limited to any particular manner of forming the gate electrodes. In addition, it is apparent that the water

10 vapor anneal can be used in any structure that includes a nitride layer, an oxynitride layer, a nitrodized oxide layer, or a nitrided oxide layer, the electrical properties of which are important to device performance. Also, it appears that the water vapor anneal step can be

15 inserted at any location(s) in the process after the formation of the dielectric layer and positive results will be achieved. This is meant to be illustrated by the different alternative locations at which the WVA steps have been inserted in the general flow diagram of the

20 fabrication process (see Fig. 1).

This technique can be applied to any device that incorporates a dielectric layer that is composed of silicon and nitrogen atoms, including amorphous and crystal SiN and silicon oxynitride. There are many ways

25 known in the art for forming such layers. For example, one might first grow a silicon oxide layer and then nitrodize the layer so as to introduce nitrogen into it (usually in amounts equal to only a few percent). Various techniques are known for nitriding the layer

30 including using N_2O , NO or NH_3 ambients. Alternatively, one might form a SiN layer (e.g. by a CVD process) and then reoxidize that layer by exposing it to an oxygen or oxygen containing ambient. Clearly the composition of

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these layers varies widely depending of course on the particular method of fabricating the layer. In general, among other things, the nitrogen serves a similar function including, for example, forming a barrier for
5 the out diffusion of dopant from the underlying material. The invention can be applied to all of these structures with similar results.

Other embodiments are within the following claims.

What is claimed is:

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Claims:

1. A method of fabricating semiconductor devices comprising the steps of:
 - forming a silicon-based dielectric layer
 - 5 containing nitrogen having a concentration that is in a range of a fraction of a percent up to stoichiometric Si_3N_4 ; and
 - annealing the dielectric layer in a water vapor atmosphere.
- 10 2. The method of claim 1 further comprising forming a gate-electrode on the dielectric layer.
3. The method of claim 2 wherein the water vapor anneal step is performed after forming said gate-electrode.
- 15 4. The method of claim 2 wherein the water vapor anneal step is performed before forming said gate-electrode.
5. The method of claim 1 wherein the dielectric layer comprises silicon nitride.
- 20 6. The method of claim 1 wherein the dielectric layer comprises a silicon oxynitride.
7. The method of claim 1 wherein the dielectric layer comprises a nitrated silicon oxide or a nitrodized silicon oxide.

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8. The method of claim 1 wherein the water vapor anneal step is performed at a temperature which is in the range of about 270°C to 500°C.

9. A semiconductor device fabricated in
5 accordance with the process of claim 1.

10. A method of fabricating semiconductor devices comprising the steps of:

forming a dielectric layer made of a material that is selected from a group of materials consisting of
10 silicon nitride, silicon oxynitride, nitrided oxide, and nitrodized oxide;

annealing the dielectric layer in a water vapor atmosphere.

11. A method of improving electrical
15 characteristics of a metal-insulator-semiconductor (MIS) device in which the insulating layer comprises a dielectric selected from the group of materials consisting of silicon nitride, silicon oxynitride, nitrided oxide, and nitrodized oxide, said method
20 comprising annealing the device in a water vapor atmosphere.

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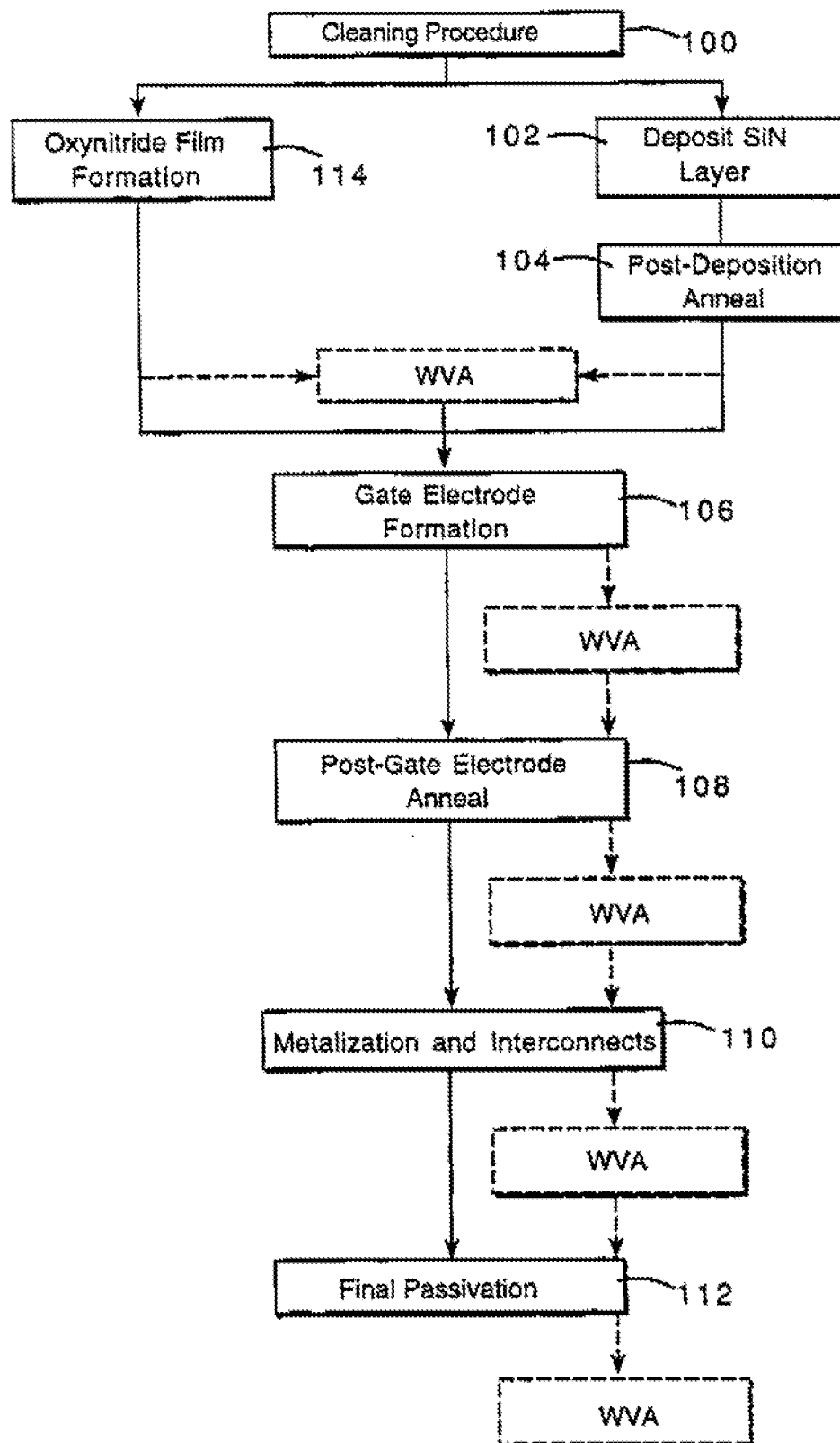


FIG. 1

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FIG. 2

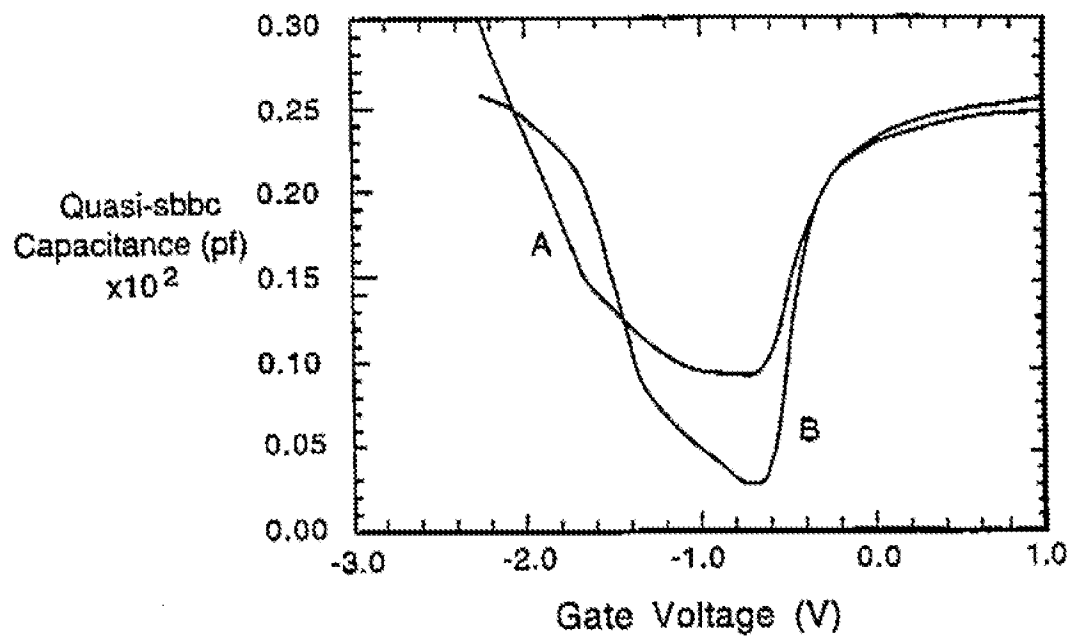
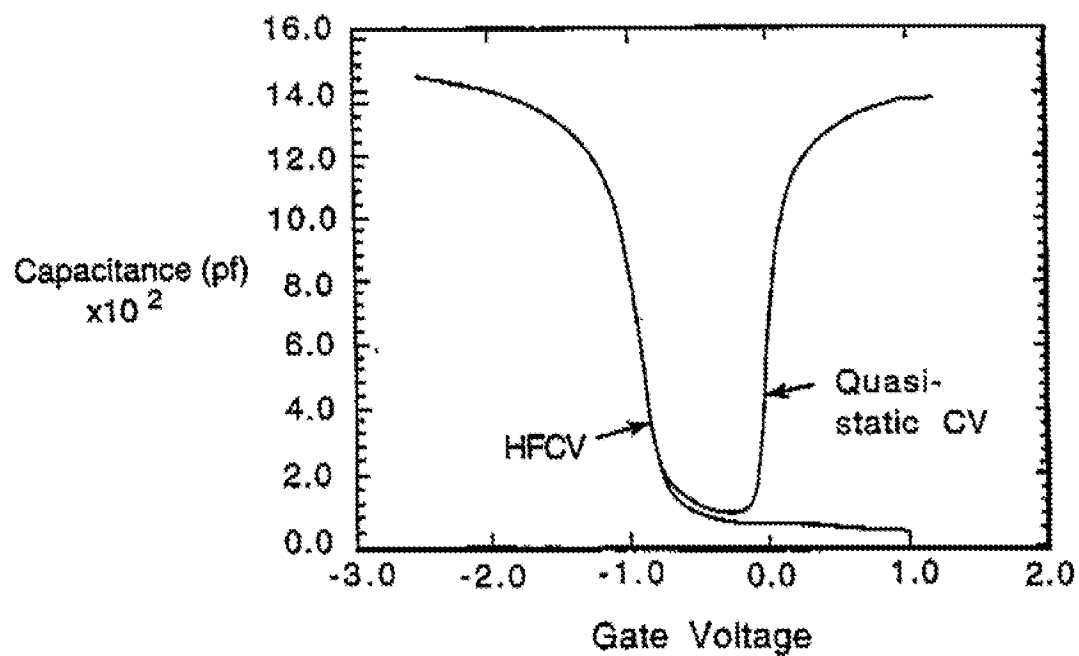


FIG. 3



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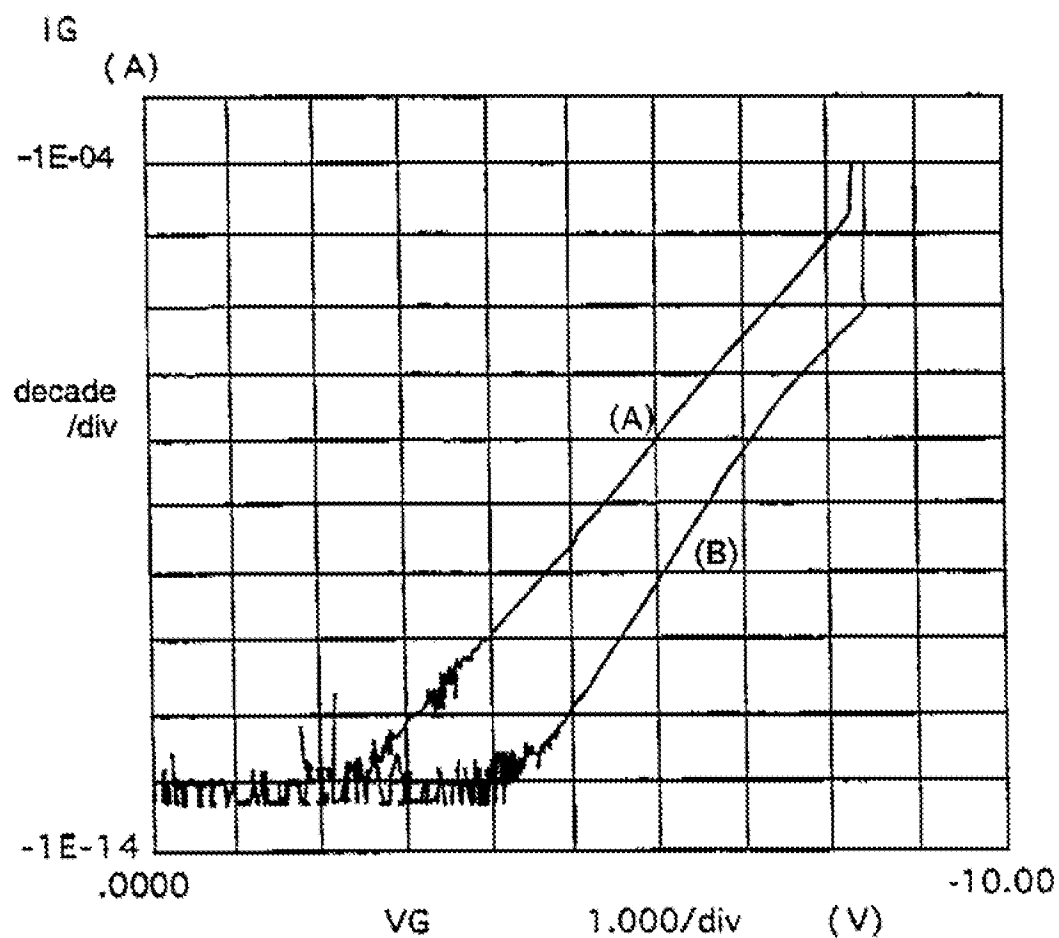
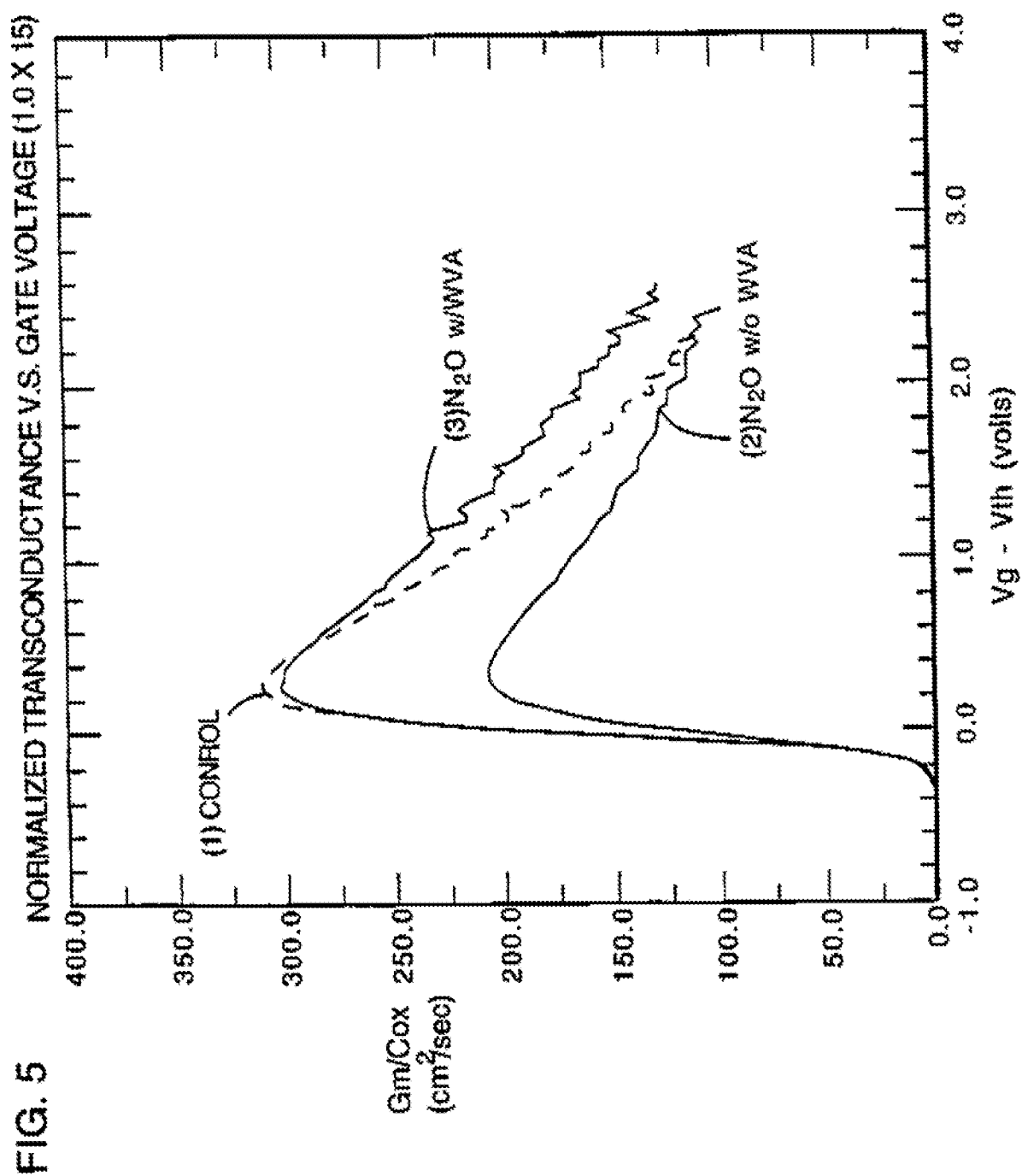
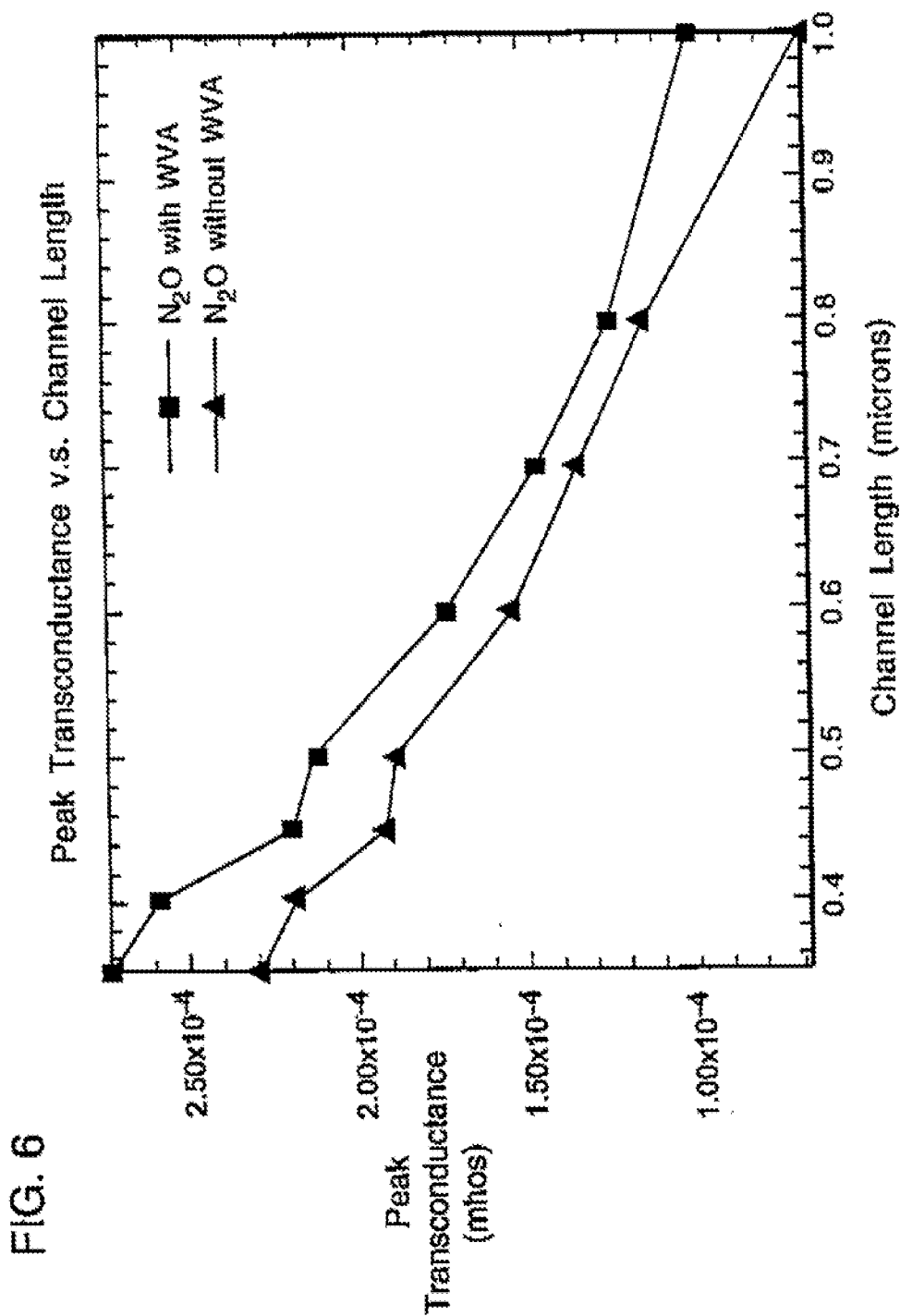


FIG. 4

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